IN THE CLAIMS

Please amend the claims to read as follows:

Claim 1 (currently amended): A method of formation of a trench vertical transistor in a semiconductor substrate having a surface and a trench with a sidewall formed in said semiconductor substrate, said semiconductor substrate being doped with a dopant, a counterdoped drain region in the surface of said substrate and a channel alongside said sidewall, said drain region having a top level and a bottom level, a counterdoped source region formed in the substrate juxtaposed with said sidewall below said channel, a gate oxide layer formed on the sidewalls of said trench, and a gate conductor formed in said trench, said method including the steps as follows:

recessing said gate conductor below said surface of said semiconductor substrate;

performing angled ion implantation at [[an]] a greater angle $\theta+\delta$ with respect to vertical of a counterdopant into said channel below the location of said drain region; and

performing angled ion implantation at [[an]] a lesser angle θ with respect to vertical of a dopant into said channel below said location of said drain region.

Claim 2 (previously presented): The method of claim 1 wherein said recessing of said gate conductor reaches below said bottom level of said drain region.

Claim 3 (currently amended): The method of claim 1 wherein the lesser angle θ is about 7° and the greater angle $\theta+\delta$ is about 30°.

Claim 4 (previously presented): The method of claim 1 wherein said counterdopant is selected from the group consisting of arsenic and phosphorus.

Claim 5 (previously presented): The method of claim 3, wherein said counterdopant comprises arsenic ion implanted at an energy of about 10 keV.

Claim 6 (currently amended): The method of claim 5 wherein the lesser angle θ is about 7° and the greater angle θ+δ is about 30°.

Claim 7 (currently amended): The method of claim 1 wherein:

said deep trench includes a deep trench capacitor; [[,]] and

said recessing of said gate conductor reaches below said bottom level of said drain region.

Claim 8 (currently amended): The method of claim 7 wherein the lesser angle θ is about 7° and the greater angle θ+δ is about 30°.

Claim 9 (currently amended): A method of formation of a deep trench vertical transistor in a semiconductor substrate having a surface and a trench with a sidewall formed in said semiconductor substrate, said deep trench including a deep trench capacitor filled with a node, a strap, a collar and a node dielectric lining said deep trench, and a buried plate formed in the semiconductor substrate surrounding said deep trench, said semiconductor substrate being doped with a dopant, a counterdoped bit line diffusion region in the surface of said substrate and a channel alongside said sidewall, said bit line diffusion region having a top level and a bottom level, a counterdoped source region formed in the substrate juxtaposed with said sidewall below said channel, a gate oxide layer formed on the sidewalls of said trench, and a gate conductor formed in said trench, said method including the steps as follows: [[r]]

recessing said gate conductor below said surface of said semiconductor substrate;

performing angled ion implantation at [[an]] a greater angle θ+δ with respect to vertical of a counterdopant into said channel below the location of said drain region; and

performing angled ion implantation at an the lesser angle δ with respect to vertical of a dopant into said channel below said location of said bit line diffusion region.

Claim 10 (previously presented): The method of claim 9 wherein said recessing of said gate conductor reaches below said bottom level of said bitline diffusion region.

Claim 11 (currently amended): The method of claim 9 wherein the lesser angle δ is about 7^{o} and the greater angle $\theta+\delta$ is about 30^{o}.

Claim 12 (previously presented): The method of claim 9 wherein said counterdopant is selected from the group consisting of arsenic and phosphorus.

Claim 13 (previously presented): The method of claim 11, wherein said counterdopant comprises arsenic ion implanted at an energy of about 10 keV.

Claim 14 (currently amended): The method of claim 12 wherein the lesser angle θ is about 7^{o} and the greater angle $\theta+\delta$ is about 30^{o}.

Claim 15 (currently amended): A method of formation of a deep trench vertical transistor in a semiconductor substrate having a surface and a deep trench with a sidewall formed in said semiconductor substrate and a bit line diffusion region juxtaposed therewith on the surface of said semiconductor substrate, comprising the steps as follows:

forming a deep trench having a top and a lower portion in a doped semiconductor substrate;

forming a counterdoped buried plate in said substrate surrounding said lower portion of said deep trench;

forming a storage node dielectric layer as a conformal thin film on inner walls of said deep trench;

filling said deep trench with an initial storage node conductor which is counterdoped;

recessing the initial storage conductor;

forming a dielectric collar as a conformal film on exposed inner walls of said deep trench with said dielectric collar recessed below said top of said deep trench;

filling said deep trench with a complementary storage node conductor which is counterdoped above and in contact with said initial storage conductor;

recessing said complementary storage node conductor to a buried strap level in said deep trench;

forming a counterdoped buried strap counterdoped outdiffusion by diffusion of dopant from said complementary storage node conductor into said substrate;

forming a trench top oxide layer over said complementary storage node conductor;

forming a gate oxide layer which is conformal with exposed inner walls of said deep trench;

forming a gate conductor in said deep trench above said trench top oxide layer;

recessing the gate conductor below the bottom surface of the bit line diffusion region, and

performing angled ion implantation at [[an]] <u>a greater</u> angle $\theta+\delta$ with respect to vertical of a counterdopant into said channel below the location of said bit line diffusion region; and

performing angled ion implantation at [[an]] <u>a lesser</u> angle θ with respect to vertical of a dopant into said channel below said location of said drain region.

Claim 16 (previously presented): The method of claim 15 wherein the lesser angle θ is about 7^{o} and the greater angle $\theta+\delta$ is about 30^{o}.

Claim 17 (previously presented): The method of claim 15 wherein said counterdopant is selected from the group consisting of arsenic and phosphorus.

Claim 18 (currently amended): The method of claim 17 wherein the lesser angle θ is about 7^{o} and the greater angle $\theta+\delta$ is about 30^{o}.

Claim 19 (previously presented): The method of claim 17, wherein said counterdopant comprises arsenic ions implanted at an energy of about 10 keV.

Claim 20 (currently amended): The method of claim 19 wherein the lesser angle θ is about 7^{o} and the greater angle $\theta+\delta$ is about 30^{o}.